In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A data transfer system comprising:

a plurality of first bus devices, at least one first bus device being a first bus data supplying device capable of supplying data, at least one first bus device being a first bus data receiving device capable of receiving data and at least one first bus device being a first bus master device capable of requesting and controlling data transfer;

a first data bus connected to each of said plurality of first bus devices and capable of transferring data from a first bus data supplying device to a first bus data receiving device under control of a first bus master device;

a plurality of second bus devices different from said plurality of first bus devices, at least one second bus device being a second bus data supplying device capable of supplying data, at least one second bus device being a second bus data receiving device capable of receiving data, a plurality of second bus devices each being a second bus master device capable of requesting and controlling data transfer, a predetermined one of said plurality of second bus devices being a dominant second bus master device;

a second data bus different from said first data bus connected to each of said plurality of second bus devices and capable of transferring data from a second bus data supplying device to a second bus data receiving device under control of a second bus master device;

a bus bridge connected to said first data bus and said second data bus, said bus bridge capable of supplying data to said first bus, receiving data from said first bus, supplying data to said second bus, receiving data from said second bus, not capable of

controlling data transfer on said first bus and capable of controlling data transfer on said second bus; and

a second bus arbiter connected to each of said at least one second bus master device, said second bus and said bus bridge, said second bus arbiter granting control of data transfer on said first bus to one and only one of the set of devices including each second bus master and said bus bridge, said second bus arbiter granting control of data transfer to said dominant second bus master immediately upon request and interrupting any data transfer controlled by another second bus master.

2. (Original) The data transfer system of claim 1, wherein:

said at least one first bus master device consists of a central processing unit.

3. (Original) The data transfer system of claim 1, wherein:

said at least one first bus master device consists of a direct memory access unit.

4. (Original) The data transfer system of claim 1, wherein:

at least one first bus supplying/receiving device consists of a memory which is not capable of controlling data transfer.

5. (Currently Amended) The data transfer system of claim 1, wherein:

each second bus master generates a corresponding bus request signal to said second bus arbiter for second bus to request control of said second bus, said second bus arbiter having grant logic corresponding to each second bus master supplying a bus grant signal to said corresponding bus master upon bus grant, said bus request signal of said dominant bus master supplied to said grant

logic corresponding to every other second bus masters for inhibiting generation of said grant request.

6. (Original) The data transfer system of claim 5, wherein:

said bus arbiter grants control of said second bus to second bus master devices other than dominant bus master in a round robin fashion.

7. (Currently Amended) ~~The~~ A data transfer system ~~of claim 1, wherein~~ comprising:

a plurality of first bus devices, at least one first bus device being a first bus data supplying device capable of supplying data, at least one first bus device being a first bus data receiving device capable of receiving data, ~~and~~ at least one first bus device being a first bus master device capable of requesting and controlling data transfer and at least one first bus supplying/receiving device ~~consists of~~ being a central processing unit which is further capable of controlling data transfer; ~~and~~

a first data bus connected to each of said plurality of first bus devices and capable of transferring data from a first bus data supplying device to a first bus data receiving device under control of a first bus master device;

a plurality of second bus devices, at least one second bus device being a second bus data supplying device capable of supplying data, at least one second bus device being a second bus data receiving device capable of receiving data, a plurality of second bus devices each being a second bus master device capable of requesting and controlling data transfer, a predetermined one of said plurality of second bus devices being a dominant second bus master device ~~said at least one second bus master device is~~ responsive to real time events asynchronous to operation of said central processing unit;

a second data bus connected to each of said plurality of second bus devices and capable of transferring data from a second bus data supplying device to a second bus data receiving device under control of a second bus master device;

a bus bridge connected to said first data bus and said second data bus, said bus bridge capable of supplying data to said first bus, receiving data from said first bus, supplying data to said second bus, receiving data from said second bus, not capable of controlling data transfer on said first bus and capable of controlling data transfer on said second bus; and

a second bus arbiter connected to each of said at least one second bus master device, said second bus and said bus bridge, said second bus arbiter granting control of data transfer on said first bus to one and only one of the set of devices including each second bus master and said bus bridge, said second bus arbiter granting control of data transfer to said dominant second bus master immediately upon request and interrupting any data transfer controlled by another second bus master.

8. (New) The data transfer system of claim 7, wherein:

said at least one first bus master device consists of a direct memory access unit.

9. (New) The data transfer system of claim 7, wherein:

at least one first bus supplying/receiving device consists of a memory which is not capable of controlling data transfer.

10. (New) The data transfer system of claim 7, wherein:

each second bus master generates a corresponding bus request signal to said second bus arbiter for second bus to request control of said second bus, said second bus arbiter having grant logic corresponding to each second bus master supplying a bus grant

signal to said corresponding bus master upon bus grant, said bus request signal of said dominant bus master supplied to said grant logic corresponding to every other second bus masters for inhibiting generation of said grant request.

11. (New) The data transfer system of claim 10, wherein:

said bus arbiter grants control of said second bus to second bus master devices other than dominant bus master in a round robin fashion.